TO THE CLAIMS

What is claimed:

1. (currently amended): A system for despreading a ~~PN code from a~~ spread spectrum signal using a PN code, wherein the spread spectrum signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the system comprising:

a switch for selecting one of the in-phase portion and the quadrature-phase portion; and

a first multiplier coupled to the switch for multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips to obtain a first product.

2. (original): The system of claim 1, further comprising:

a second multiplier coupled to the switch for multiplying the selected portion of a second of the plurality of signal samples with the one of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples; and

a first adder coupled to the first multiplier and the second multiplier for adding the first product with the second product to obtain a first sum.

3. (original): The system of claim 2, further comprising:

a third multiplier coupled to the switch for multiplying the selected portion of a third of the plurality of signal samples with a second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips;

a fourth multiplier coupled to the switch for multiplying the selected portion of a fourth of the plurality of signal samples with the second of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples;

a second adder coupled to the third multiplier and the fourth multiplier for adding the third product with the fourth product to obtain a second sum; and

a third adder coupled to the first adder and the second adder for adding the first sum with the second sum.

4. (original): The system of claim 1, further comprising:

a second multiplier coupled to the switch for multiplying the selected portion of a second of the plurality of signal samples with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

a first adder coupled to the first multiplier and the second multiplier for adding the first product with the second product to obtain a first sum.

5. (original): The system of claim 4, further comprising:

a third multiplier coupled to the switch for multiplying the selected portion of a third of the plurality of signal samples with the second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples;

a fourth multiplier coupled to the switch for multiplying the selected portion of a fourth of the plurality of signal samples with a third of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples and wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

a second adder coupled to the third multiplier and the fourth multiplier for adding the third product with the fourth product to obtain a second sum; and

a third adder coupled to the first adder and the second adder for adding the first sum with the second sum.

6. (currently amended): A method for despreading ~~a PN code from a~~ spread spectrum signal using a PN code, wherein the spread spectrum signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the method comprising:

selecting one of the in-phase portion and the quadrature-phase portion; and

multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips to obtain a first product.

7. (original): The method of claim 6, further comprising:

multiplying the selected portion of a second of the plurality of signal samples with the one of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples; and

adding the first product with the second product to obtain a first sum.

8. (original): The method of claim 7, further comprising:

multiplying the selected portion of a third of the plurality of signal samples with a second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips;

multiplying the selected portion of a fourth of the plurality of signal samples with the second of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples;

adding the third product with the fourth product to obtain a second sum; and

adding the first sum with the second sum.

9. (original): The method of claim 6, further comprising:

multiplying the selected portion of a second of the plurality of signal samples with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples and

wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

adding the first product with the second product to obtain a first sum.

10. (original): The method of claim 9, further comprising:

multiplying the selected portion of a third of the plurality of signal samples with the second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples;

multiplying the selected portion of a fourth of the plurality of signal samples with a third of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples and wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

adding the third product with the fourth product to obtain a second sum; and

adding the first sum with the second sum.

11. (original): A computer data signal embodied in a carrier wave comprising:

(a) a receiving source code segment comprising means for receiving a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion; and

(b) a processing source code segment comprising:

(i) means for selecting one of the in-phase portion and the quadrature-phase portion; and

(ii) means for multiplying the selected portion of one of the plurality of signal samples with one of a plurality of PN code chips to obtain a first product.

12. (original): The computer data signal of claim 11, wherein the processing source code segment further comprises:

(iii) means for multiplying the selected portion of a second of the plurality of signal samples with the one of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples; and

(iv) means for adding the first product with the second product to obtain a first sum.

13. (original): The computer data signal of claim 12, wherein the processing source code segment further comprises:

(v) means for multiplying the selected portion of a third of the plurality of signal samples with a second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips;

(vi) means for multiplying the selected portion of a fourth of the plurality of signal samples with the second of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples;

(vii) means for adding the third product with the fourth product to obtain a second sum; and

(viii) means for adding the first sum with the second sum.

14. (original): The computer data signal of claim 11, wherein the processing source code segment further comprises:

(iii) means for multiplying the selected portion of a second of the plurality of signal samples with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

(iv) means for adding the first product with the second product to obtain a first sum.

15. (original): The computer data signal of claim 14, wherein the processing source code segment further comprises:

(v) means for multiplying the selected portion of a third of the plurality of signal samples with the second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples;

(vi) means for multiplying the selected portion of a fourth of the plurality of signal samples with a third of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of

signal samples and wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

(vii) means for adding the third product with the fourth product to obtain a second sum; and

(viii) means for adding the first sum with the second sum.

16. (currently amended): A computer readable medium having software for despreading a ~~PN code from a~~ spread spectrum signal using a PN code, wherein the spread spectrum signal comprises a plurality of signal samples, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the computer readable medium comprising:

means for selecting one of the in-phase portion and the quadrature-phase portion; and

means for multiplying the selected portion of one of the plurality of signal samples with one of the plurality of PN code chips to obtain a first product.

17. (original): The computer readable medium of claim 16, further comprising:

means for multiplying the selected portion of a second of the plurality of signal samples with the one of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples; and

means for adding the first product with the second product to obtain a first sum.

18. (original): The computer readable medium of claim 17, further comprising:

means for multiplying the selected portion of a third of the plurality of signal samples with a second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips;

means for multiplying the selected portion of a fourth of the plurality of signal samples with the second of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples;

means for adding the third product with the fourth product to obtain a second sum; and

means for adding the first sum with the second sum.

19. (original): The computer readable medium of claim 16, further comprising:

means for multiplying the selected portion of a second of the plurality of signal samples with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal samples succeeds the one of the plurality of signal samples and wherein the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

means for adding the first product with the second product to obtain a first sum.

20. (original): The computer readable medium of claim 19, further comprising:

means for multiplying the selected portion of a third of the plurality of signal samples with the second of the plurality of PN code chips to obtain a third product, wherein the third of the plurality of signal samples succeeds the second of the plurality of signal samples;

means for multiplying the selected portion of a fourth of the plurality of signal samples with a third of the plurality of PN code chips to obtain a fourth product, wherein the fourth of the plurality of signal samples succeeds the third of the plurality of signal samples and wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

means for adding the third product with the fourth product to obtain a second sum; and

means for adding the first sum with the second sum.

21. (currently amended): A system for despreading a ~~PN code from a~~ spread spectrum signal using a PN code, wherein the spread spectrum signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the system comprising:

a first switch for selecting one of the in-phase portion and the quadrature-phase portion;

a second switch coupled to the first switch for selecting one of the even sample and the odd sample; and

a first multiplier coupled to the second switch for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips to obtain a first product.

22. (original): The system of claim 21, further comprising:

a second multiplier coupled to the second switch for multiplying the selected portion of the selected sample of a second of the plurality of signal sample pairs with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal sample pairs succeeds the one of the plurality of signal sample pairs, and the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

an adder coupled to the first multiplier and the second multiplier for adding the first product with the second product to obtain a first sum.

23. (original): The system of claim 22, further comprising:

a third multiplier coupled to the second switch for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the one of the plurality of PN code chips to obtain a third product;

a fourth multiplier coupled to the second switch for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a fourth product;

a second adder coupled to the third multiplier and the fourth multiplier for adding the third product with the fourth product to obtain a second sum; and

a third adder coupled to the first adder and the second adder for adding the first sum with the second sum.

24. (original): The system of claim 22, further comprising:

a third multiplier coupled to the second switch for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a third product;

a fourth multiplier coupled to the second switch for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with a third of the plurality of PN code chips to obtain a fourth product, wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

a second adder coupled to the third multiplier and the fourth multiplier for adding the third product with the fourth product to obtain a second sum; and

a third adder coupled to the first adder and the second adder for adding the first sum with the second sum.

25. (currently amended): A method for despreading a ~~PN code from a~~ spread spectrum signal using a PN code, wherein the spread spectrum signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the method comprising:

selecting one of the in-phase portion and the quadrature-phase portion;

selecting one of the even sample and the odd sample; and

multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips to obtain a first product.

26. (original): The method of claim 25, further comprising:

multiplying the selected portion of the selected sample of a second of the plurality of signal sample pairs with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal sample pairs succeeds the one of the plurality of signal sample pairs, and the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

adding the first product with the second product to obtain a first sum.

27. (original): The method of claim 26, further comprising:

multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the one of the plurality of PN code chips to obtain a third product;

multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a fourth product;

adding third product with the fourth product to obtain a second sum; and

adding the first sum with the second sum.

28. (original): The method of claim 26, further comprising:

multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a third product;

multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with a third of the plurality of PN code chips to obtain a fourth product, wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

adding third product with the fourth product to obtain a second sum; and

adding the first sum with the second sum.

29. (original): A computer data signal embodied in a carrier wave comprising:

(a) a receiving source code segment comprising means for receiving a spread spectrum signal, wherein the spread spectrum signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion; and

(b) a processing source code segment comprising:

(i) means for selecting one of the in-phase portion and the quadrature-phase portion;

(ii) means for selecting one of the even sample and the odd sample; and

(iii) means for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of a plurality of PN code chips to obtain a first product.

30. (original): The computer data signal of claim 29, wherein the processing source code segment further comprises:

(iv) means for multiplying the selected portion of the selected sample of a second of the plurality of signal sample pairs with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal sample pairs succeeds the one of the plurality of signal sample pairs, and the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

(v) means for adding the first product with the second product to obtain a first sum.

31. (original): The computer data signal of claim 30, wherein the processing source code segment further comprises:

(vi) means for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the one of the plurality of PN code chips to obtain a third product;

(vii) means for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a fourth product;

(viii) means for adding the third product with the fourth product to obtain a second sum; and

(ix) means for adding the first sum with the second sum.

32. (original): The computer data signal of claim 30, wherein the processing source code segment further comprises:

(vi) means for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a third product;

(vii) means for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with a third of the plurality of PN code chips to obtain a fourth product, wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

(viii) means for adding the third product with the fourth product to obtain a second sum; and

(ix) means for adding the first sum with the second sum.

33. (currently amended): A computer readable medium having software for despreading ~~a PN code from a~~ spread spectrum signal using a PN code, wherein the spread spectrum signal comprises a plurality of signal sample pairs, each pair comprising an even signal sample and an odd signal sample, each signal sample having an in-phase portion and a quadrature-phase portion, and wherein the PN code comprises a plurality of chips, the computer readable medium comprising:

means for selecting one of the in-phase portion and the quadrature-phase portion;

means for selecting one of the even sample and the odd sample; and

means for multiplying the selected portion of the selected sample of one of the plurality of signal sample pairs with one of the plurality of PN code chips to obtain a first product.

34. (original): The computer readable medium of claim 33, further comprising:

means for multiplying the selected portion of the selected sample of a second of the plurality of signal sample pairs with a second of the plurality of PN code chips to obtain a second product, wherein the second of the plurality of signal sample pairs succeeds the one of the plurality of signal sample pairs, and the second of the plurality of PN code chips succeeds the one of the plurality of PN code chips; and

means for adding the first product with the second product to obtain a first sum.

35. (original): The computer readable medium of claim 34, further comprising:

means for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the one of the plurality of PN code chips to obtain a third product;

means for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a fourth product;

means for adding the third product with the fourth product to obtain a second sum; and

means for adding the first sum with the second sum.

36. (original): The computer readable medium of claim 34, further comprising:

means for multiplying the selected portion of the other sample of the one of the plurality of signal sample pairs with the second of the plurality of PN code chips to obtain a third product;

means for multiplying the selected portion of the other sample of the second of the plurality of signal sample pairs with a third of the plurality of PN code chips to obtain a fourth product, wherein the third of the plurality of PN code chips succeeds the second of the plurality of PN code chips;

means for adding the third product with the fourth product to obtain a second sum; and

means for adding the first sum with the second sum.

37-65. (canceled)